	FYBSC IT SEM-II				
	Subject: Microprocessor architecture				
Sr.No	**Question**	**A**	**B**	**C**	**D**
	Unit One				
1	Microprocessor was introduced in the year_____	1945	1971	1974	1980
2	Flip – flops are used in a microprocessor to indicate_____	Shift register	latches	counters	flags
3	The number of address lines required to access 64 Kbyte of memory	16	32	20	8
4	Flip –flops are used in a microprocessor to indicate	shift register	latch	counters	flag
5	The first microprocessor was _____	4001	8085	4003	4004
6	Which of the following microprocessor has an 8 bit data	4004	80186	8085	8086
7	The number of flags in 8085 are _____	4	8	6	5
8	A microprocessor is _____	a. an analog device	b. a digital device	c. an analog and digital	d. none of these
9	The 16 bit processor is _____	8085	b.8086	c.80486	d. pentium
10	The data bus of microprocessor is _____	unidirectional	bi –directional	unidirectional as well as bi	none of these
11	Which system communicates with the outside word via the I/O devices	Microprocessor	Microcomputer	Digital computer	All of these
12	How many generation of microprocessor:	Four	Five	Six	Three
13	Each machine cycle consists of many clock periods called	t-states	instruction cycle	fetch cycle	machine cycle
14	The length of LXI H, 9000H is _____	one-byte	two-byte	three-byte	four-byte
15	Why 8085 processor is called an 8 bit processor?	because 8085 processor has 8	because 8085 processor has 8	because 8085 processor has	because 8085 processor has 16
16	The address / data bus in 8085 is _____.	multiplexed	demultiplexed	decoded	encoded
17	In 8085 name the 16 bit registers?	Stack pointer	Program counter	Both a and b	None of these
18	In 8085, 16-bit address bus, which can address upto?	16KB	32KB	64KB	128KB
19	machine language instruction format consist of	Operation code field	Operation code field &	Operand field	none of the mentioned
20	Assembly language programs are written using	Hex code	Mnenonics	ASCII code	None of these View
21	How many types of Interfacing?	2	3	4	5

Unit Two				
STA 4000 is --------byte instruction	one	three	two	four
RAL is an example of ----------addressing mode	register	direct	implied	immediate
Stack pointer is a -------- register	16 bit	8 bit	32 bit	4bit
In memory mapped I/O device is identified by	8bit address	IN instruction16bit address		OUT instruction
In I/O mapped input device is	latch	buffer	decoder	stack
In I/O mapped output device is	buffer	encoder	latch	stack
If accumulator content is 88H, after execution of CMA accumulator	77H	93H	FFH	80H
LDA is ---------Instruction	arithmetic	logical	branch	data transfer
If A=56H,B=82H after execution of ANA B ,content of A= -----	02H	56H	00H	D8H
8085 has EPROM of	1Kb	526bytes	64kb	256 bytes
In 8085, 16-bit address bus, which can address upto?	16KB	32KB	64KB	128KB
There are _____ general purpose registers in 8085 processor	5	6	7	8
It is also a 16-bit register works like stack, which is always	Stack pointer	Temporary register	Flag register	Program counter
Flag register is an 8-bit register having _____ 1-bit flip-flops.	3	4	5	6
What is true about Program counter?	It is an 8-bit register, which	When an instruction is fetched	It provides timing and	It is a 16-bit register used to
This signal indicates that another master is requesting the use of the	READY	HOLD	HLDA	INTA
This signal is used as the system clock for devices connected with the	X1, X2	CLK OUT	CLK IN	IO/M
Which of the following is true about Control and status signals?	These signals are used to	There are 3 control signal and 3	Three status signals are	All of the above
The register in the 8085A that is used to keep track of the memory	stack pointer	program counter	instruction pointer	accumulator
The data bus in 8080A/8085 microprocessor is a group of	eight bidirectional lines that are	sixteen bidirectional lines that	eight unidirectional lines that	eight lines used to transfer data
In 8085, to disable the whole interrupt system (except TRAP)	the DI instruction may be used	the DO instruction may be used	the INTERRUPT instruction	the El instruction may be used
Exceptions to the 8085 microprocessor normal operation are called:	jump instructions	decoding	interrupts	jump instructions or interrupts
In 8085 microprocessor, which of the following interrupts has the	RST 5.5	RST 7.5	TRAP	INTR
Which of the following was not a design improvement for the	Execution unit (EU)	16-bit data bus	Arithmetic logic unit (ALU)	Bus interface unit (BIU)
How many buses are connected as part of the 8085A microprocessor?	2	3	5	6
Unit Three				

	Unit Three				
51	In which of these modes, the immediate operand is included in the	register operand mode	immediate operand mode	register and immediate operar	none of the mentioned
52	In register address mode, the operand is stored in	8-bit general purpose register	16-bit general purpose register	si or di	all of the mentioned
53	A sequence of two registers that multiplies the content of DE register	XCHG & DAD B	XTHL & DAD H	PCHL & DAD D	XCHG & DAD H
54	The accumulator contains 85H, register B contains 68H, what is the	35H, 1	53H, 0	35H, 0	53H, 1
55	Which instruction is required to rotate the content of accumulator one	RLC	RAL	RRC	RAR
56	The accumulator contains 03H and register D containd 81H, what is the	83H, 0	38H, 0	83H, 1	38H, 1
57	Register pair used to indicate memory	B and C	D and E	H and L	W and Z
58	What are software interrupts?	RST 0-7	RST 5.5 - 7.5	INTR, TRAP	RST 4.4 - 6.4
59	For one's complement following instruction is use	CMA	CMP	CMC	CMT
60	For Exchanging data following instruction is used	Exchange	XCHG	Change	EXCH
61	checking for errors in the program by oberving the execution of	Static debugging	Reg debugging	Dynamic debugging	A & C
62	The time required for the execution of the program depends on ___	t-states	instruction cycle	fetch cycle	machine cycle
63	There are ____ many tools are available for dynamic debugging	2	4	5	3
64	_____ instruction use to adjust result to BCD	DAD	DDA	DAA	ADA
65	CMA	calculate 1's complement	calculate 2's complement	addition	complement
66	DAD B means	HL+BC	H+B	L+C	D+B
67	SBB B instruction says	A-B-Borrow	B-B	B-B-Borrow	A & B
68	what is the content of the accumulator and the CY after	21H, 1	12H, 0	21H, 0	12H, 1
69	To generate a delay using 8 bit counter	MVI D, Count	MOV D, Count	MVI D, Count	MOV D, Count
70	What is the length of the temporary register of 8085 microprocessor?	32 bits	12 bits	16 bits	8 bits
71	How many I/O ports can be accessed by direct method in 8085 microprocessor	8	128	256	64
72	How many I/O ports can be accessed by memory mapped method in of 8085 microprocessor?	8K	32K	256K	64K
73	What is the addressing mode used in instruction MOVE M, C ?	Direct	Induced	Indirect	Immediate

84		**Unit Four**				
85	76	In BCD to Binary Code Converter MS digit is multiplied by	0A	0B	0C	0F
86	77	DAA command stands for _____	Divide Accumulator Arithmetic	Decimal Accumulator Arithmeti	Divide Adjust Accumulator	Decimal Adjust Accumulator
87	78	_____ is a tool that converts assembly language program to	Accumulator	Debbuger	Assembler	Code Converter
88	79	The 8085 microprocessor has _____ hardware interrupts.	4	5	6	7
89	80	_____ has highest priority among all interrupts	RST 7.5	RST 6.5	INTR	TRAP
90	81	INTR interrupt is pin number _____ in pin diagram of 8085	7	8	9	10
91	82	ISR address or Vector location for TRAP is	002C	003C	0024	0034
92	83	There are _____ software interrupts	8	7	6	5
93	84	_____ intruction is not masking/unmasking of interrupts	EI	MVI	RIM	SIM
94	85	What is SIM in context of microprocessor ?	Select Interrupt Mask	Sorting Interrupt Mask	Set Interrupt Mask	Set Integer Mask
95	86	What is meant by maskable interrupts?	an interrupt which can never be	an interrupt that can be turned	an interrupt which can never	an interrupt which can never be
96	87	In 8085 microprocessor address line for RST3 is ?	0020H	0028H	0018H	0019H
97	88	RIM is used to check whether, _____	The write operation is done or	The interrupt is Masked or not	a & b	None of these
98	89	Storage which stores or retains data after power off is called-	Volatile storage	Non-volatile storage	Sequential storage	Direct storage
99	90	Which of the following memories must be refreshed many times per	EPROM	ROM	Static RAM	Dynamic Ram
100	91	Which device is used to back up the data?	Floppy Disk	Tape	Network Drive.	All of the above
101	92	What is the permanent memory built into your computer called?	RAM	ROM	CPU	CD-ROM
102	93	The two basic types of memory in a computer are _____	Primary and major	Primary and Secondary	Minor and Major	Main and virtual
103	94	A non-erasable disk that stores digitized audio information is ____	CD	CD-ROM	DVD-R	DVD-RW
104	95	Magnetic tape is not practical for applications where data must be	A random-access medium	A sequential-access medium	A read-only medium	An expensive storage medium
105	96	Hard disc drives are considered.....storage-	Flash	Non-volatile	Temporary	Non-permanent
106	97	_____ is a set of small program that are designed to operate major PC	BIOS	CIOS	AIOS	None of these
107	98	Which of the following system software resides in the main memory alw	Text editor	Assembler	Linker	Loader
108	99	By whom address of external function in the assembly source file suppli	Assembler	Linker	Machine	Code
109	100	which of the 2 files are created by the assembler:	List and object file	Link and object file	Both a & b	None of these

	Unit Five				
101	The Pentium memory system is divided into	4 banks	8 banks	6 banks	10 banks
102	Return CPU Identification code is carried out by the instruction	CPUID	CPID	COPID	RCPID
103	The Pentium Pro microprocessor has provisions for a ----- address bus	32 bit	64 bit	36 bit	63 bit
104	The---------instruction is used by external circuitry to request an	INRT	INTR	NIRT	NITR
105	A new feature added to the Pentium and Pentium Pro is the capability	purity	parity	errors	sum
106	Which is an instruction set architecture?	Pentium	Sun microsystems	Core processor	SPARC
107	In ------mode, the processor can execute any instruction, including the	admin	monitor	supervisor	user
108	A -------- is induced by a particular instruction and occurs before any	precise trap	trap	deffered trap	exception trap
109	The Pentium 4 and Core2 microprocessors require a modified ----------	AXT power supply	TAX power supply	ATX power supply	XTA power supply
110	This significant advancement combines two microprocessors into a	Hyper technology	Multi processor technology	Combination technology	Hyper threading technology
111	The CISC stands for _____	Computer Instruction Set Compli	Complete Instruction Set Compl	Computer Indexed Set Compo	Complex Instruction set computer
112	The computer architecture aimed at reducing the time of execution of ins	CISC	RISC	ISA	ANNA
113	The Sun micro systems processors usually follow _____ architecture.	CISC	ISA	ULTRA SPARC	RISC
114	Pipe-lining is a unique feature of _____	RISC	CISC	ISA	IANA
115	In CISC architecture most of the complex instructions are stored in ___	Register	Diodes	CMOS	Transistors
116	What does SPARC stand for?	scalable processor architecture	speculating architecture	speculating processor	scaling Pentium architecture
117	Which company developed SPARC?	intel	IBM	Motorola	sun microsystem
118	How many external interrupts does SPARC processor support?	5	10	15	20
119	How many instructions does SPARC processor have?	16	32	64	128
120	When an external interrupt is generated, what type of mode does the pro	real mode	virtual mode	protected mode	supervisor mode
121	Which module of SPARC contains the general purpose registers?	IU	FPU	CU	control unit
122	Who introduced Pentium family?	intel	wipro	cts	samsung
123	Dual independent bus architecture was first introduced in the	pentium pro processor	pentium II processor	pentium III processor	pentium IV processor
124	The processor 80386/80486 and the Pentium processor uses _____	16	32	36	64
125	In which year, Pentium pro processor introduced?	1996	1998	1995	1999

Consider the following memory values and a one-address machine with an accumulator, what values do the following instructions load into accumulator?

- Word 20 contains 40
- Word 30 contains 50
- Word 40 contains 60
- Word 50 contains 70

Instructions are-

1. Load immediate 20
2. Load direct 20
3. Load indirect 20
4. Load immediate 30
5. Load direct 30
6. Load indirect 30

105) The register section is related to_____ of the computer:

a. Processing

b. ALU

c. Main memory

d. None of these

106) In Microprocessor one of the operands holds a special register called:

lculator

Dedicated

Accumulator

None of these

107) Which register is a temporary storage location:

general purpose register

dedicated register

A and B

ne of these

108) PC stands for:

Program counter

ints counter

Paragraph counter

Paint counter

113) How many parts of single address computer instruction :

2

3

4

114) Single address computer instruction has two parts:

The operation code

The operand

A and B

ne of these

115) LA stands for:

Load accumulator

ast accumulator

Last accumulator

None of these

116) Which are the flags of status register:

Over flow flag

117) The carry is operand by:

Carry flag

c

Half carry flag

D

Zero flag

S

terrupt flag

O

Negative flag

118) The sign is operand by:

All of these

s

D

C

O

119) The zero is operand by:

121) _____ Stores the instruction currently being executed:

Instruction register

Current register

Both a and b

ne of these

132) The left side of any binary number is called:

Least significant digit

Most significant digit

dium significant digit

low significant digit

133) MSD stands for:

Least significant digit

Most significant digit

dium significant digit

low significant digit

WE stands for:

Write enable

Wrote enable

ite envy

None of these

144) MAR stands for:

Memory address register

Memory address recode

cro address register

None of these

145) MDR stands for:

Memory data register

Memory data recode

cro data register

None of these

DMA stands for:

a. Direct memory access

b. Direct memory allocation

c. Data memory access

d. Data memory allocation

148) The ____ place the data from a register onto the data bus:

a. CPU

b. ALU

c. Both A and B

d. None of these

151) The external device is connected to a pin called the _____ pin on the processor chip.

Interrupt

ansfer

Both

None of these

152) Which interrupt has the highest priority?

INTR

Trap

RST6.5

none of these

153) In 8085 name the 16 bit registers?

Stack pointer

program counter

a & b

none of these

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