SYBSC IT Subject :-EMBEDDED SYSTEM (SEM-IV)

Sr.No	Question	A	B	C	D
	Unit One				
1	What is CISC?	Computing instruction set complex	Complex instruction set computing	Complementary instruction set computing	Complex instruction set complementary
2	It retains its content when power is remove What type of memory is this?	Volatile memory	Non-volatile memory	RAM	SRAM
3	What kind of visual panel is used for seven segmented display?	LED	LCD	Binary output	Analogue output
4	An embedded system is a combination of ----------	hardware, software, memory	hardware, firmware, mechanical components	hardware, system bus, memory	Cpu, i/o and memory
5	An embedded system can do ----------task	multi task at a time	single task at a time	specific task	all the above.
6	Embedded systems are ----------	general purpose	special purpose	domain purposes	all the above
7	An embedded system must have	hard disk	processor and memory	operating system	processor and input-output unit(s)
8	Which of the following is not an example of a 'Small scale embedded System'?	Electronic Barbie doll	simple calculator	Cell phone	Electronic toy car
9	Which of the following is (are) an intended purpose(s) of embedded systems?	Data Collection	Data Processing	Data Communication	all of these
10	Which of the following is an (are) example(s) of embedded system for data communication?	USB Mass storage device	Network router	Digital camera	Music player
11	Little Endian Processor means	Store the lower order byte of the data at the lowest address and the higher order byte of the data at the highest address memory	Store the higher-order byte of the data at the lowest address and the lower order-byte of the data at the highest address of memory	Store both higher order and lower order byte of the data at the same address of memory	Store both higher order and lower byte of the data at the higher address of memory
12	The instruction set of RISC processor is	Simple and lesser in number	complex and lesser in number	Simple and larger in number	Complex and larger in number
13	Which characteristics of an embedded system exhibit the responsiveness to the assortments or variations in system's environment by computing specific results for real-time applications without any kind of postponement ?	Single-functioned Characteristic	Tightly-constraint Characteristics	Reactive & Real time Characteristics	All of the above

14	Match the following registers with their functions : Line Status Register ---------- 1. Set Up the communication parameters Line Control Register ---------- 2. Sharing of similar addresses Transmit & Receive Buffers ---------- 3. Status Determination of Tx & Rr	A-2, B-1, C-3	A-1, B-2, C-3	A-3,B-1, C-2	A-3, B-2, C-1
15	What is the directional nature of two active wires SDA & SCL usually adopted in I2C Bus for carrying the information between the devices ?	Uni-directional	Bi-directional	Multi-directional	None of the above
16	Which potential mode of operation indicate the frequent sending of byte to the slave corresponding to the reception of an acknowledge signal when it becomes desirable for the master to write to the slave during data transmission in I2C bus?	Master in master-transmit mode & Slave in slave-receive mode	Slave in slave-transmit mode & Master in master-receive mode	Master in master-transmit mode as well as master-receive mode	Slave in slave-transmit mode as well as slave-receive mode
17	Which among the below stated salient feature/s of SPI contribute to the wide range of its applicability?	Simple hardware interfacing	Full duplex communication	Low power requirement	All of the above
18	Which kind of assembler do not generate the programs in similar language as that used by micro-controllers by developing the program in high-level languages making them as machine independent?	Macro Assembler	Cross Assembler	Meta Assembler	All of the above
19	Which development tool / program has the potential to allocate the specific addresses so as to load the object code into memory?	Loader	Locator	Library	Linker
20	The assembler list file generated by an assembler mainly includes _____	binary codes	assembly language statements	offset for each instruction	all of the above
21	Which architectural scheme has a provision of two sets for address & data buses between CPU and memory?	Harvard architecture	Von-Neumann architecture	Princeton architecture	All of the above
22	which is/are the operational quality attribute?	Response	Throughput	Reliability	All of the above
23	which is/are the non- operational quality attribute?	Testability and Debug-ability	safety	security	reliability
24	_____deals with the possible damage that can happen to the operating person and environment due to the breakdown of an embedded system or due to the emission of hazardous materials from the embedded products.	Testability and Debug-ability	safety	security	reliability
25	Confidentiality, Integrity and Availability are three corner stones of _____	Testability and Debug-ability	safety	security	reliability
	Unit Two				
26	Name a volatile memory.	RAM	EPROM	ROM	EEPROM
27	Which one of the following is UV erasable?	Flash memory	SRAM	EPROM	DRAM
28	How the input terminals are associated with external environments?	Actuators	Sensors	Inputs	Outputs
29	Why is SRAM more preferably in non-volatile memory?	low-cost	high-cost	low power consumption	transistor as a storage element
30	_____ is a ISO defined serial communication bus originally developed for the automotive industry.	CAN	LAN	WAN	MAN

32	_____ is the processor's address book.	memory map	IO map	Interrupt map	Polling
33	The _____ is the function called when a particular interrupt occurs.	IRS	ISR	IRR	ISS
34	_____ method simply uses a code sectio which checks a particular flag or status of operation	memory map	IO map	Interrupt map	Polling
35	A nonvolatile type of memory that can be programmed and erased in sectors, rather than one byte at a time is:	Flash memory	PROM	EPROM	ROM
36	Memory that doesnt loses its contents when power is lost is:	Volatile memory	Non-volatile memory	A and B	None of these
37	What is meant by the term RAM?	Memory which only be rea	Memory which both read and written	Memory which is used for	Memory which can only be written
38	The two kind of main memory are	primary and secondary	direct and sequential	floppy disk and hard disk	None of these
39	Which of the following memories below is often used in typical computer operation?	SRAM	DRAM	HDD	FDD
40	What is the name given to the memory which works on time sharing principle in order to create an illusion of infinite memory space?	Flash memory	Virtual Memory	Cache memory	ROM
41	DMA stands for _____	Direct Memory Access	Depend Memory Access	Data Memory Access	Data Memory address
42	_____ is a specific checksum algorithm that is designed to detect the most common data errors.	CRC	CRR	CCR	RCR
43	_____ ia a electronic timer that is used to detect and recover from computer malfunction	Watchdog Timer	COP timer	watchdog	All of the above
44	There are _____ types of watchdog timer	2	3	4	5
45	_____ is amethod of transferring data from the computer's RAM to another part of the computer without processing it using the CPU.	DMA	DMM	AMD	DAM
46	There are _____ types of Hybrid memory devices	2	3	4	5
47	PROM is also called as _____	FPROM	OTPNVM	A and B	None of these
48	Each storage location of EPROM consist of a single _____	FET	Diode	Gate	None of these
49	EDO, SD, DDR are types of _____	RAM	ROM	Flash	Cache
50	In response to specific event the microcontroller stops executing main code and switches to a different section called as _____	ISR	ISS	IRR	IRS
	Unit Three				
51	The internal RAM memory of the 8051 is:	32 bytes	64 bytes	128 bytes	256 bytes
52	The 8051 has _____ 16-bit counter/timers.	1	2	3	4
53	The 8051 can handle _____ interrupt sources.	3	4	5	6
54	When the 8051 is reset and the line is HIGH, the program counter points to the first program instruction in the	internal code memory	external code memory	internal data memory	external data memory
55	An alternate function of port pin P3.4 in the 8051 is:	Timer 0	Timer 1	interrupt 0	interrupt 1
56	The I/O ports that are used as address and data for external memory are	ports 1 and 2	ports 1 and 3	ports 0 and 2	ports 0 and 3
57	Microcontrollers often have:	CPUs	RAM	ROM	all of the above
58	The 8051 has _____ parallel I/O ports.	2	3	4	5

59	The total external data memory that can be interfaced to the 8051 is:	32K	64K	128K	256K
60	Which of the following is not an addressing mode of 8051?	register instructions	register specific instructions	indexed addressing	none of the above
61	_____ is used to transfer data between microprocessor and I/O process.	8255A	8279	8254A	8237A
62	8051 series has how many 16 bit registers?	2	3	1	0
63	When 8051 wakes up then 0x00 is loaded to which register?	DPTR	SP	PC	PSW
64	When the micro controller executes some arithmetic operations, then the flag bits of which register are affected?	PSW	SP	DPTR	PC

65	How is the status of the carry, auxiliary carry and parity flag affected if write instruction
	MOV A,#9C
	ADD A,#64H
		CY=0,AC=0,P=0	CY=1,AC=1,P=0	CY=0,AC=1,P=0	CY=1,AC=1,P=1

66	How many bytes of bit addressable memory is present in 8051 based micro controllers?	8 bytes	32 bytes	16 bytes	128 bytes
67	JZ, JNZ, DJNZ, JC, JNC instructions monitor the bits of which register ?	DPTR	B	A	PSW
68	What is the meaning of the instruction MOV A,05H ?	data 05H is stored in the accumulator	fifth bit of accumulator is set to one	address 05H is stored in the accumulator	none of the mentioned
69	To initialise any port as an output port what value is to be given to it?	0xFF	0x00	0x01	A port is by default an output port
70	Which of the following registers are not bit addressable?	SCON	PCON	A	PSW
71	There is/are ____ ways to create a time dealy in 8051C	Using a simple For Loop	Using 8051 timers	only A	both A and B
72	Packed BCD 0x29 what will be unpacked BCD?	0x02,0x09	0x20,0x90	0x0209	0x0902
73	An alternate function of port pin P3.0 (RX in the 8051 is:	serial port input	serial port output	memory write strobe	memory read strobe
74	8051 has _____ register Bank.	2	3	4	5
75	Memory addresses from 80H to FFH is allocated to _____.	Bit addressable registers	SFR	general purpose register	Register Bank
	Unit Four				
76	Which system software is used to convert a "C" language program in to language ofanother processor?	Compiler	Linker	Cross compiler	Cross Linker
77	Embedded C programming language support _____ instructions of normal "C"language	All	Some	Specific	None
78					
79	Cross Compiler converts	Program into C language into binary language	Programming C language into another language.	Program in C language into program of another processors language	Both A & B
80	____ is the function of system can be changed or upgraded by changing the software or replacing one IC with another one without incurring a heavy additional cost.	Compatibility	Size	Availability	Functionality Testing
81	COFF stands for	Common Object File Format	Center object file format	Compiling object file	none of these
82	The job of _____ is mainly to translate human readable program into equivalent set of opcodes.	Compiler	Linker	Cross compiler	Cross Linker

83	uninitialized global variables in a section called as_____	gcc	text	data	bss
84	All of the code blocks are collected into a section called_____	gcc	text	data	bss
85	The job of _____ is to combine all object files and in the process to resolve all of the unresolved symbols.	Compiler	Linker	Cross compiler	Cross Linker
86	The tool that performs the conversion from relocatable program to executable binary image is called a _____	Compiler	Linker	Cross compiler	Locator
87	COFF is also known as _____	executable file	Linable Format file	A and B	None of these
88	The code to be run on the target embedded system is called as _____	binary executable code	hex code	A and B	None of these
89	The process of putting this code in the memory chip of the target embedded system is called _____	Downloading	Uploading	compiling	Linking
90	An _____ provides a lot more functionality than a remote debugger.	ICE	CIE	ECI	IDD
91	A _____ can be used to download, execute and debug embedded software over a serial port or network connection between host and target.	Cross Compiler	Remote Linker	Remote Debugger	Remote compiler
92	What does ICE stand for?	in-circuit emulation	in-code EPROM	in-circuit EPOM	in-code emulation
93	Which of the following is a traditional method for emulating the processor?	SDS	ICE	CPU simulator	Low-level language simulator
94	_____ is the process of eliminating the bugs / errors in software	Downloading	Uploading	compiling	Debugging
95	These is/are the way/ways of doenloading the binary image on the embedded system	Using a Device Programmer	Using in system programmer	A and B	None of these
96	A debug monitor is also called as _____	RAM Monitor	ROM Monitor	target Monitor	None of these
97	A_____ is a piece of laboratory equipment designed specifically for troubleshooting digital hardware.	Emulators	Simulators	logic analyzer	Remote Debugger
98	_____ can be used as a strating program in embedded system.	Hello world	Blinking LED	7 segment display	stepper motor
99	CRO stands for _____	Cathode Ray Oscilloscope	Current Resistance Oscillator	Central Resistance Oscillator	Capacitance Resistance Oscilloscope
100	C.R.O gives _____	actual representation	visual representation	approximate representation	incorrect representation
	Unit Five				
101	List the important considerations when selecting a processor.	Instruction set	Maximum bits in an operand	Clock frequency	all of the above
102	Final stage software is also called as _____ image	ROM	RAM	EPROM	EEPROM
103	An IDE also known as _____	Intergrated design environment	Intergrated debugging environment	A and B	none of the above
104	There are _____phases to Product development	2	3	4	5
105	_____involves understanding what product needs to be developed	Analysis	Design	Implementation	Testing
106	_____ involves what approach to be used to build the product	Analysis	Design	Implementation	Testing
107	_____ is developing the product by realizing the design.	Analysis	Design	Implementation	Testing

108	_____is the process of launching the first fully functional model of the product in the market.	Analysis	Design	testing	Deployment
109	_____phase deals with the operational and maintenance of the product in the production environment.	Design	testing	Deployment	Support
110	This phase is the final phase in a product development life cycle where the product is declared as discontinued from the market.	Retirement	testing	Deployment	Support
111	The _____ is the repetitive process in which the Waterfall model is repeated over and over to correct the ambiguities observed in each iteration.	iterative model	Waterfall model	Prototyping Model	Spiral Model
112	In this _____the Product development starts with project definition and traverse through all phases of EDLC(Embedded Product Development Life Cycle).	iterative model	Waterfall model	Prototyping Model	Spiral Model
113	Embedded systems are being designed on single silicon chip called as _____	SSC	SoC	SCC	SCO
114	OMA stands for_____	open mobile alliance	object mobile alliance	opcode mobile alliance	None of the mentioned
115	_____ is a single board microcontroller, proposed to make the application of interactive objects.	DSP	Arduino	ASIP	SoC
116	ARM processor are_____	Advanced RISC Machine	above RISC Machine	About RISC machine	None of the mentioned
117	Which of the following conditions must be satisfied to solve the critical section problem?	Mutual Exclusion	Progress	Bounded Waiting	All of the mentioned
118	The segment of code in which the process may change common variables, update tables, write into files is known as _____	program	critical section	non – critical section	synchronizing
119	Which of the following is not the state of a task?	New	Old	Waiting	Running
120	Process synchronization of programs is done by	input	output	operating system	memory
121	Which scheduling algorithm allocates the CPU first to the process that requests the CPU first?	first-come, first-served scheduling	shortest job scheduling	priority scheduling	none of the mentioned
122	Which algorithm is defined in Time quantum?	shortest job scheduling algorithm	round robin scheduling algorithm	priority scheduling algorithm	multilevel queue scheduling algorithm
123	What is a medium-term scheduler?	It selects which process has to be brought into the ready queue	It selects which process has to be executed next and allocates CPU	It selects which process to remove from memory by swapping	None of the mentioned
124	What is a short-term scheduler?	It selects which process has to be brought into the ready queue	It selects which process has to be executed next and allocates CPU	It selects which process to remove from memory by swapping	None of the mentioned
125	What is a long-term scheduler?	It selects which process has to be brought into the ready queue	It selects which process has to be executed next and allocates CPU	It selects which process to remove from memory by swapping	None of the mentioned